



# Self-Aligned Quadruple Patterning Made Simple

Extending the Applications of Atomic Layer Etch-induced Pitch Splitting (APS™)

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- Start Up & Spin-Off from Lund University.
- Founded in Lund, Sweden 2019.
- Strong team of 14 experts.

## Managed by experts in ALE and semiconductor equipment



**Jonas Sundqvist, PhD**

**CEO & Co-founder**

- Developed ALD and CVD processes since 1999
- Over >25 years' experience in semiconductor manufacturing
- Passionate entrepreneur who delivers on promises
- Strong network in semiconductor market



**Robin Athle, PhD**

**R&D Manager**

- APS™ process lead
- Expert in emerging memories, semiconductor devices and materials



**Dmitry Suyatin, PhD**

**CSO & Co-founder**

- Over 15 years of experience in advanced processing of nanostructures
- Author of more than 30 publications
- Well-known ALE expert in ecosystem



**Peo Hansson**

**Advisor Semi Equipment**



**Amin Karimi, PhD**

**CTO & Co-founder**

- Hands-on experience in Nanofabrication
- Expert in semiconductor devices and materials



**Garry Miner**

**Advisor Semi Equipment**



**Per-Anders Eriksson**

**Deputy CEO and COO**

- Business Development
- Semiconductor Equipment industry



**Robert Cadman,**

**Advisor Business Development**



## **ALE Pitch Splitting - APS™**

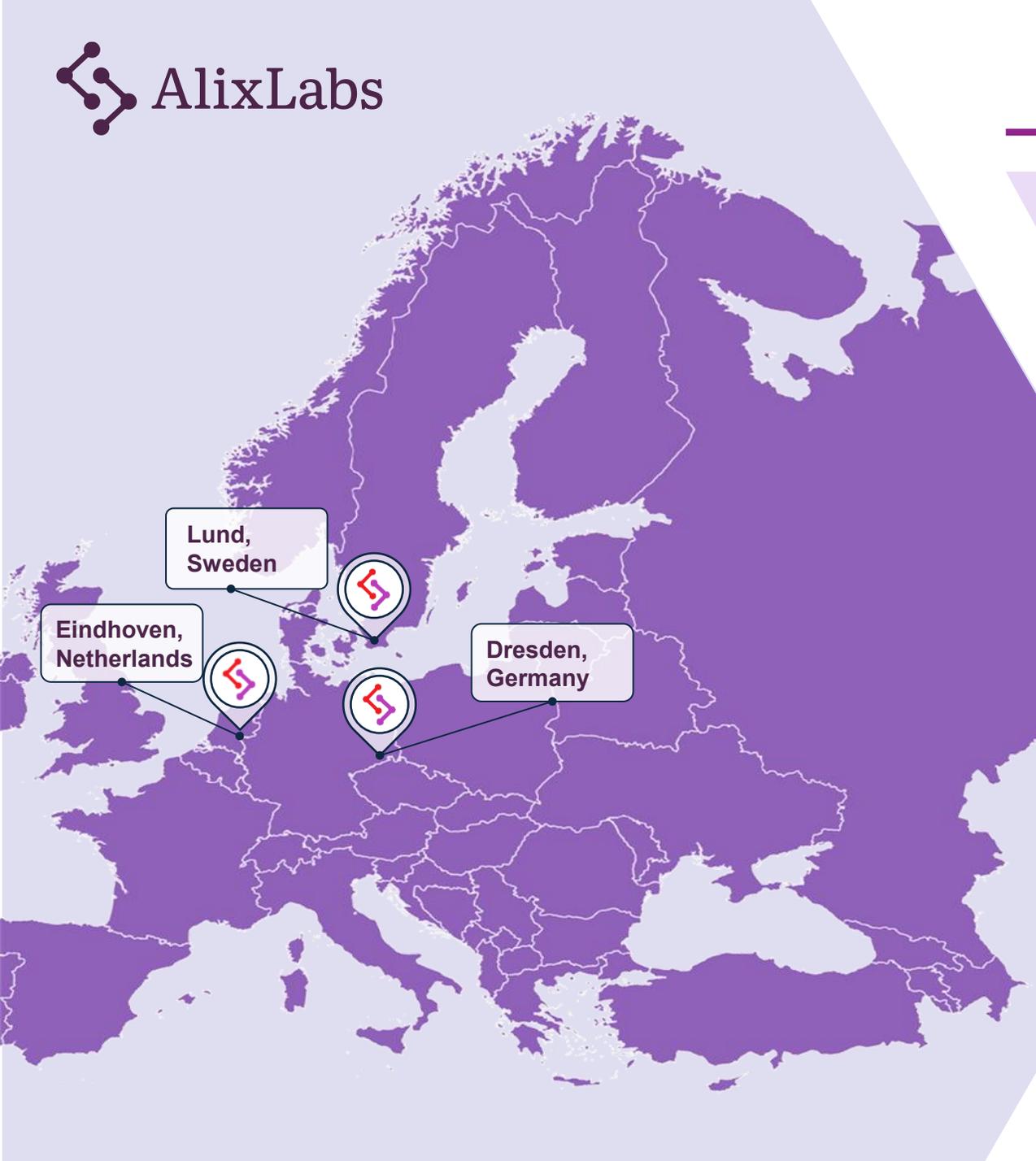
Enabling advanced node size scaling. Enhancing performance and efficiency.

## **ALE for Power Electronics**

Specialized ALE applications for III-Vs, GaN and SiC.

## **ALE Equipment**

First 300 mm ALE equipment provider in Sweden.



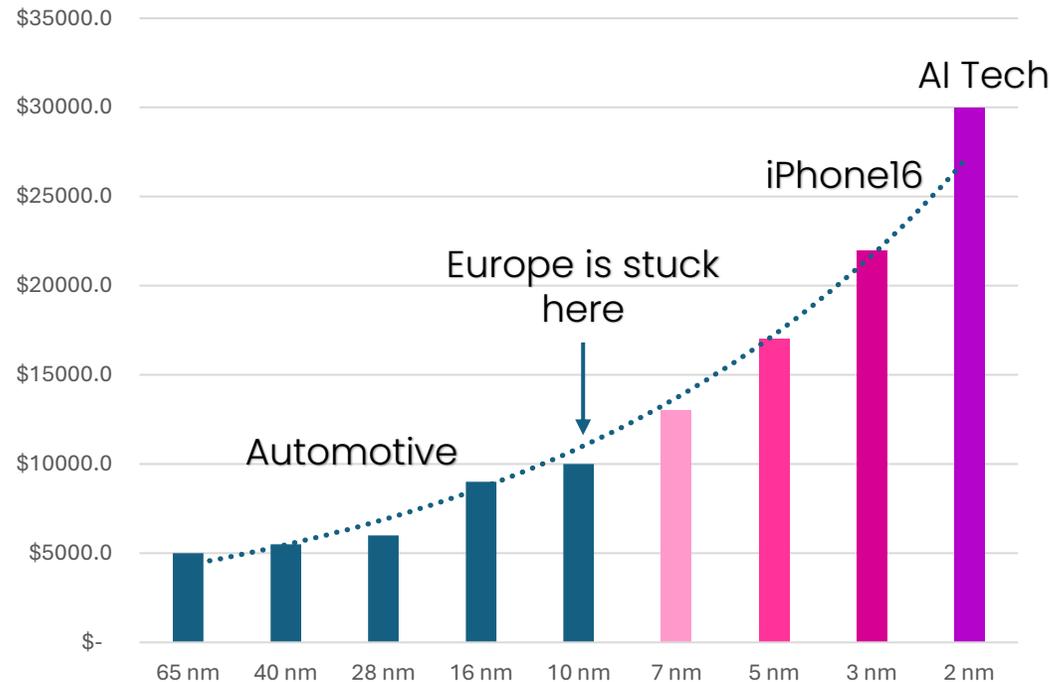
Eindhoven,  
Netherlands

Lund,  
Sweden

Dresden,  
Germany

# Escalating manufacturing costs challenge the industry as demand for smaller nodes continues to rise

## Wafer price (\$)



Source: TSMC Wafer Price by manufacturing node, The Information Network

Node Size (nm)

Wafer prices are increasing at an unsustainable rate, driven by consumer applications such as AI.

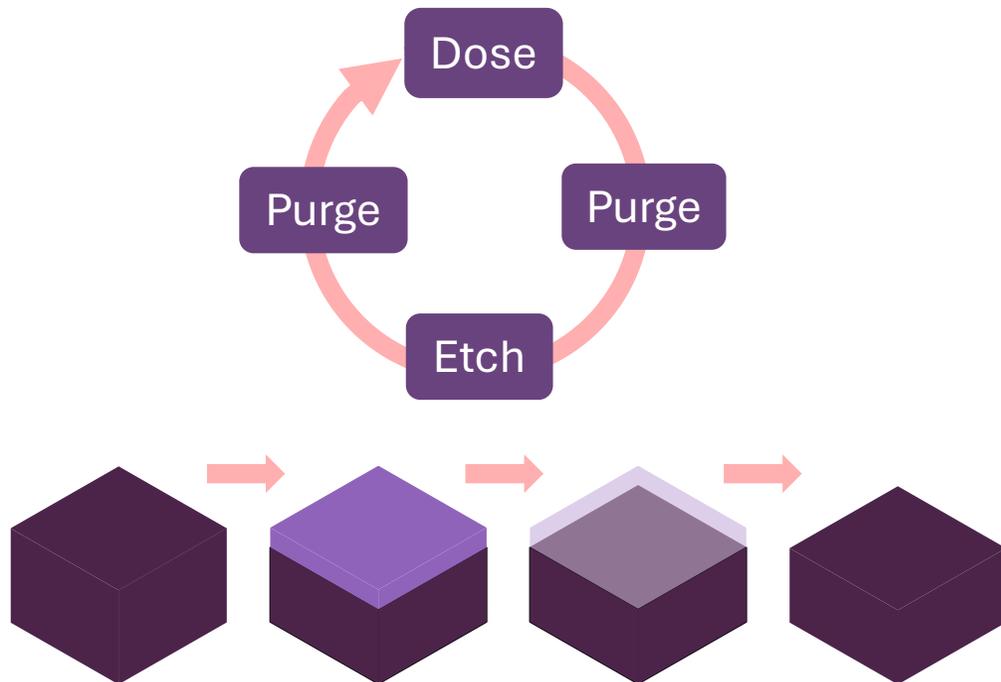
The exploding wafer price is due to rising process complexity, especially advanced patterning using EUV or multi-patterning schemes (LELE / SADP / SAQP).

Every extra lithography and etch step increases cost, variability and integration risk. Is there a better way?

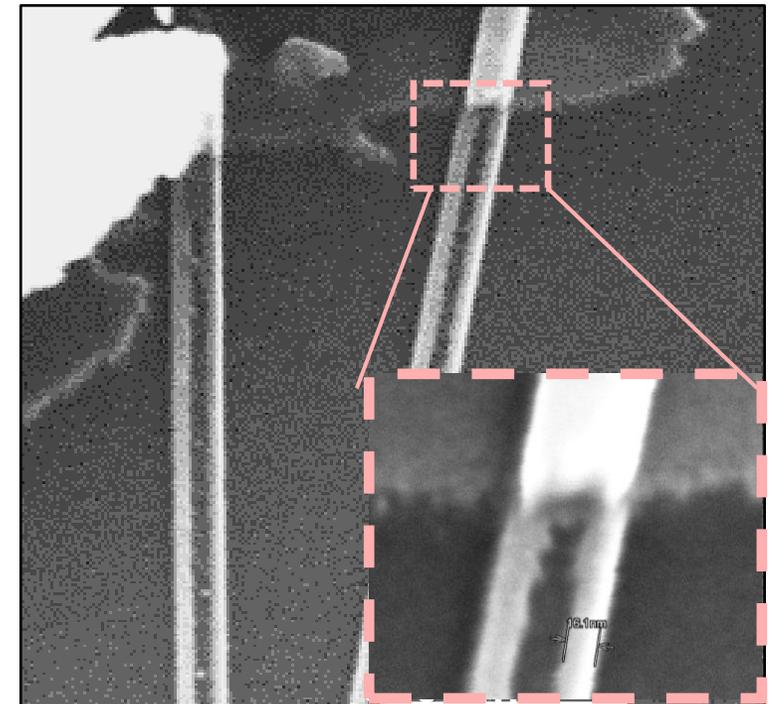
**The million dollar questions: Can we reduce pitch and CD without multiplying lithography steps?**

# Atomic Layer Etching & Pitch Splitting

**Atomic Layer Etching (ALE) -The inverse of ALD.** Atomic level surface control using self-limiting chemistries.



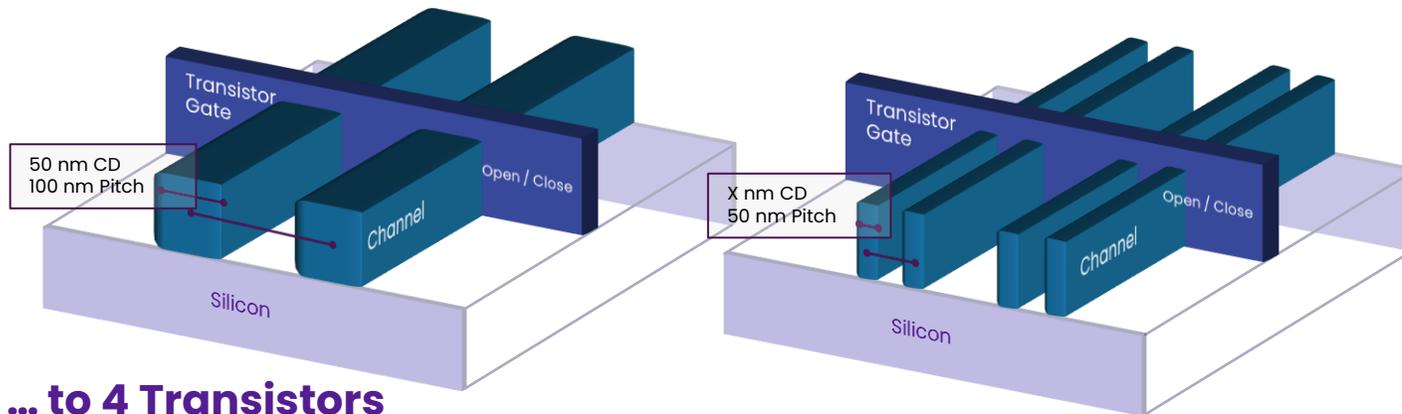
**Atomic Layer Etch Pitch Splitting (APS™)** – First demonstration in 2016 of GaP Nanowires on Si.



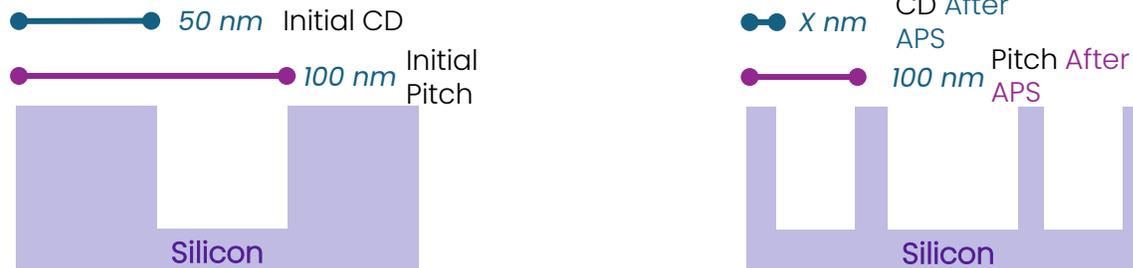
Pitch and CD reduction without additional lithography or deposition!

# APS™ Doubles On-chip Feature Density

## From 2 Transistors



## ... to 4 Transistors

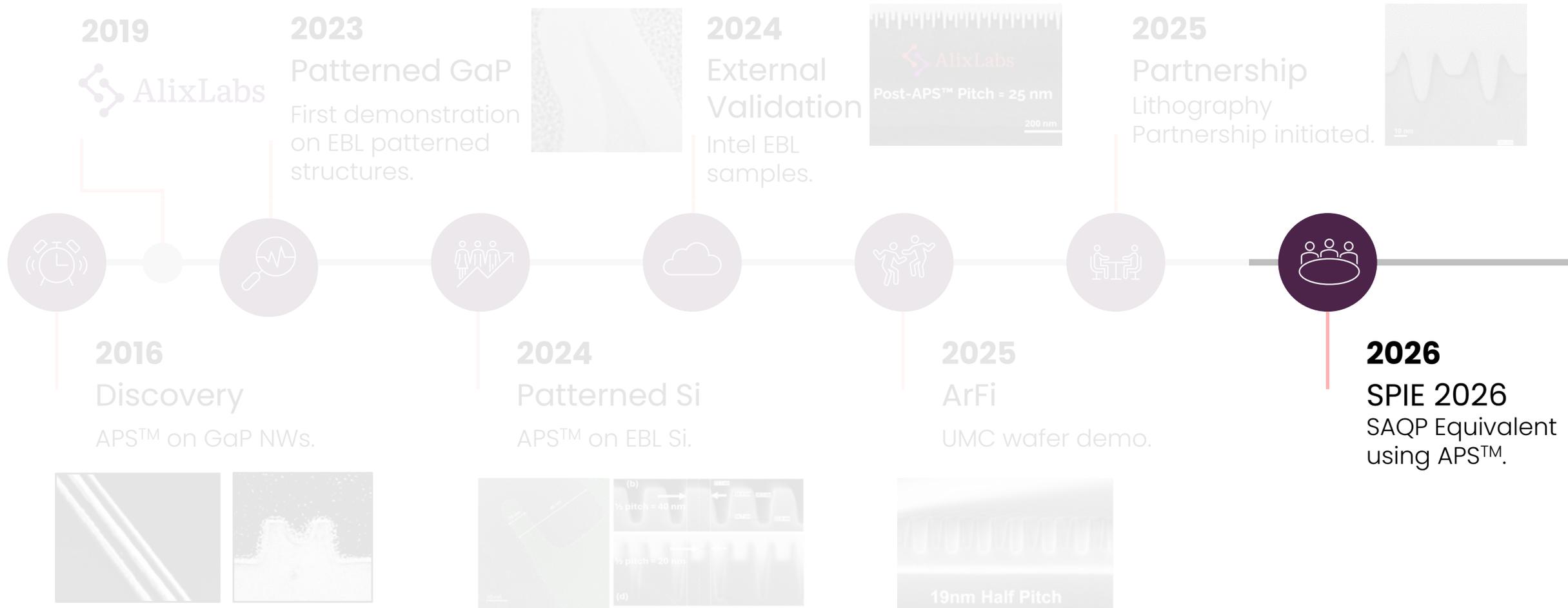


**Without additional lithography or deposition!**

- APS™ allows for a doubling of fins on chip without any additional lithography or deposition process.
- More transistors per chip allows for increased compute.
- APS™ offers reduced complexity and improved sustainability compatible with current fab equipment.
- Advanced process nodes without investing in expensive EUV.



# APST™ Development Timeline



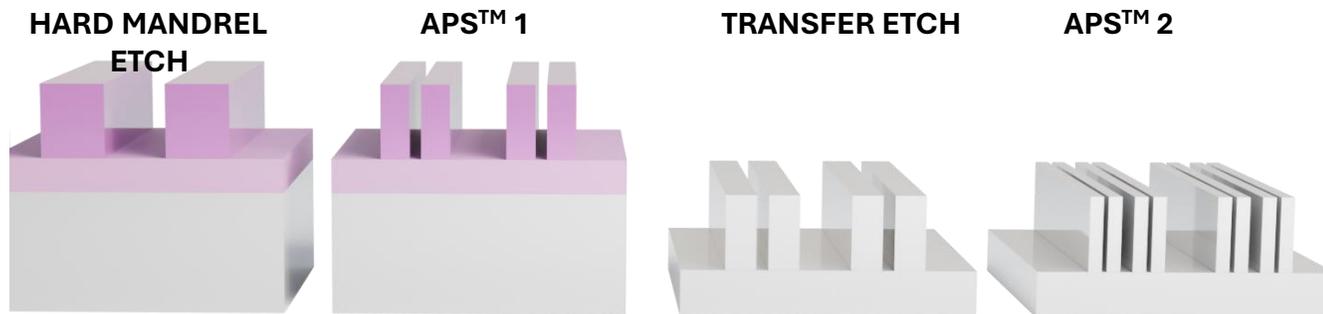
# Comparing SAQP with APS™

## Simplified SAQP Process Flow

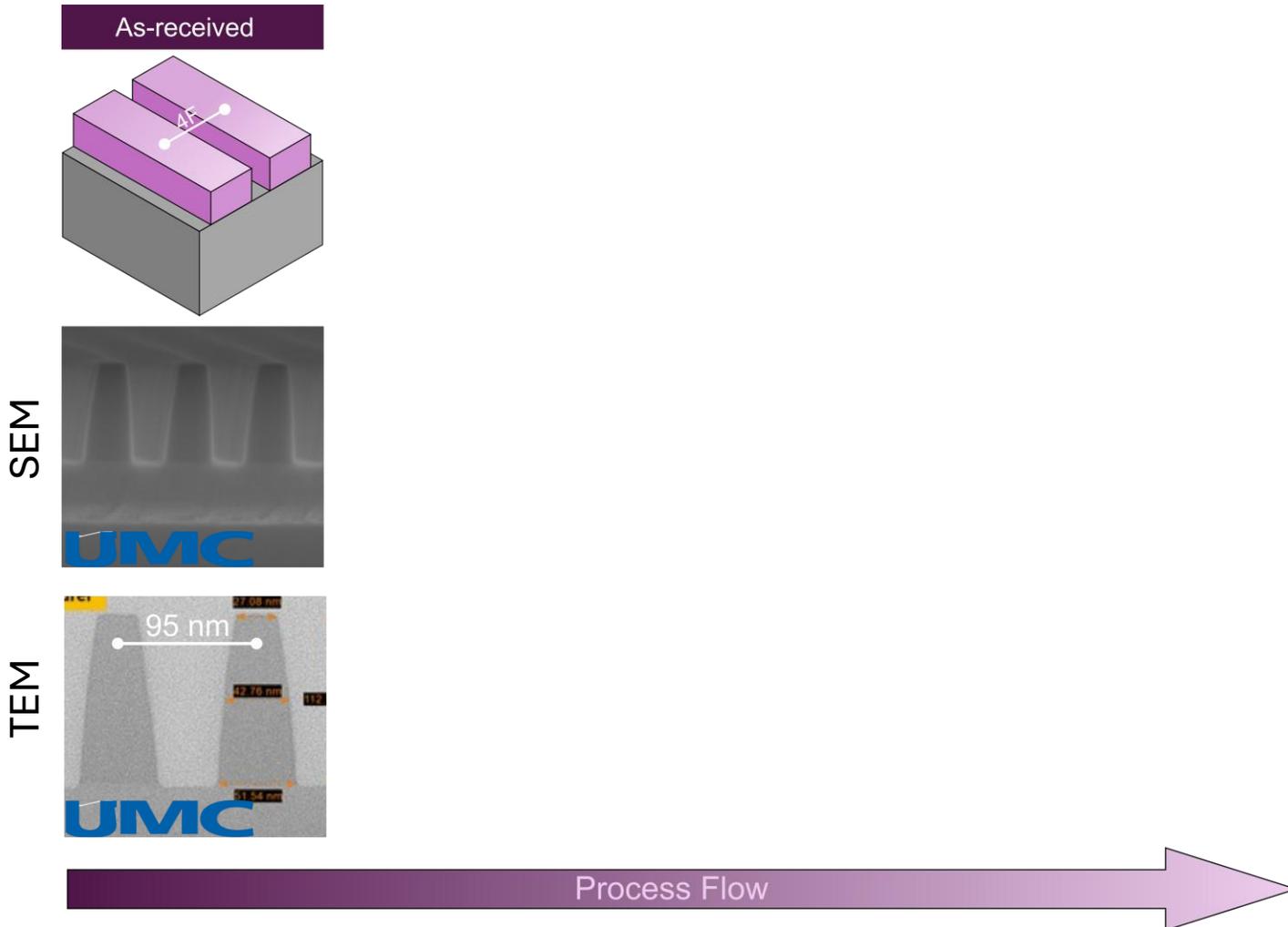


*E. Altamirano-Sánchez et al, SPIE Newsroom (2016)*

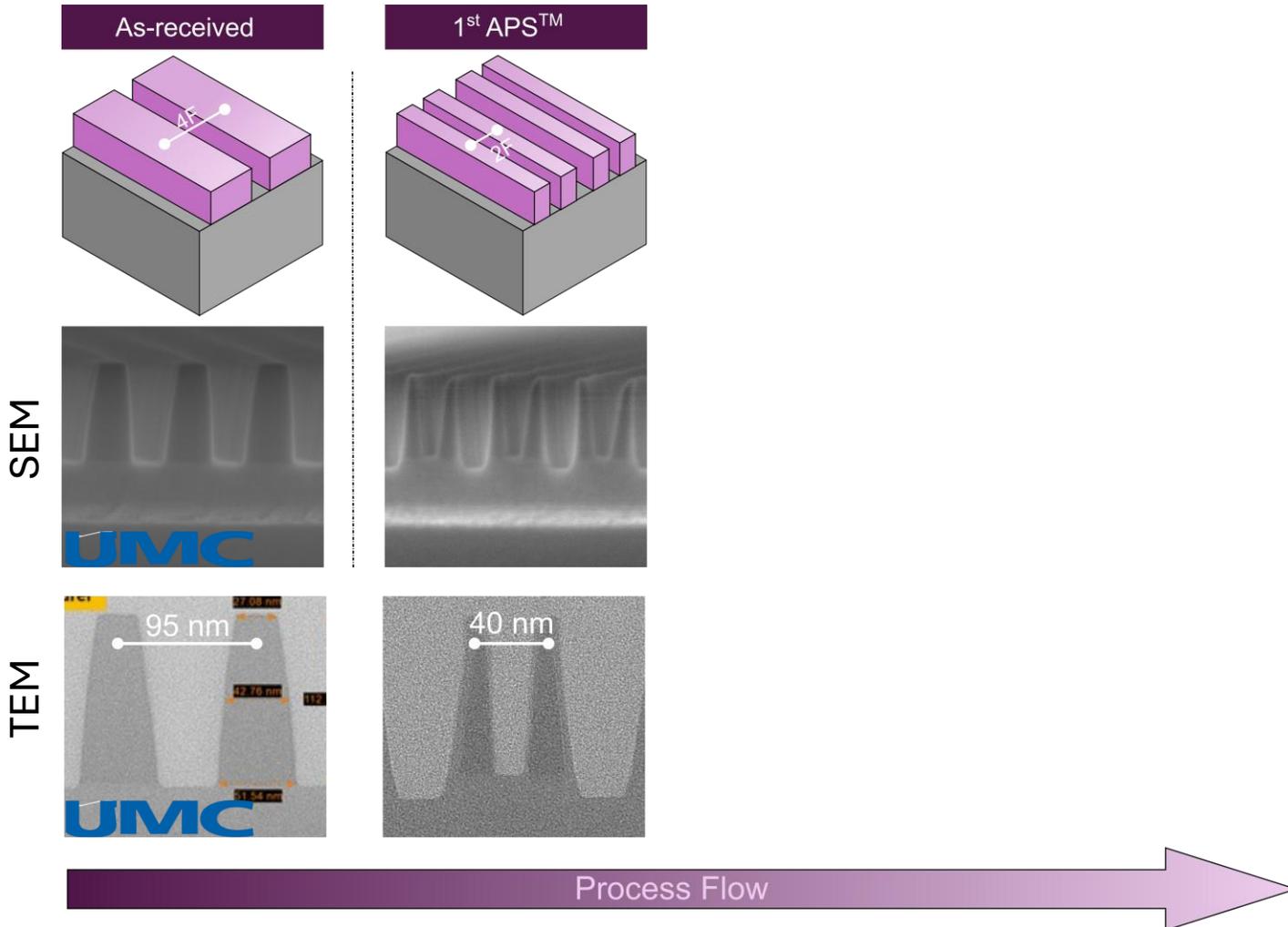
## APS™ Pitch Quartering



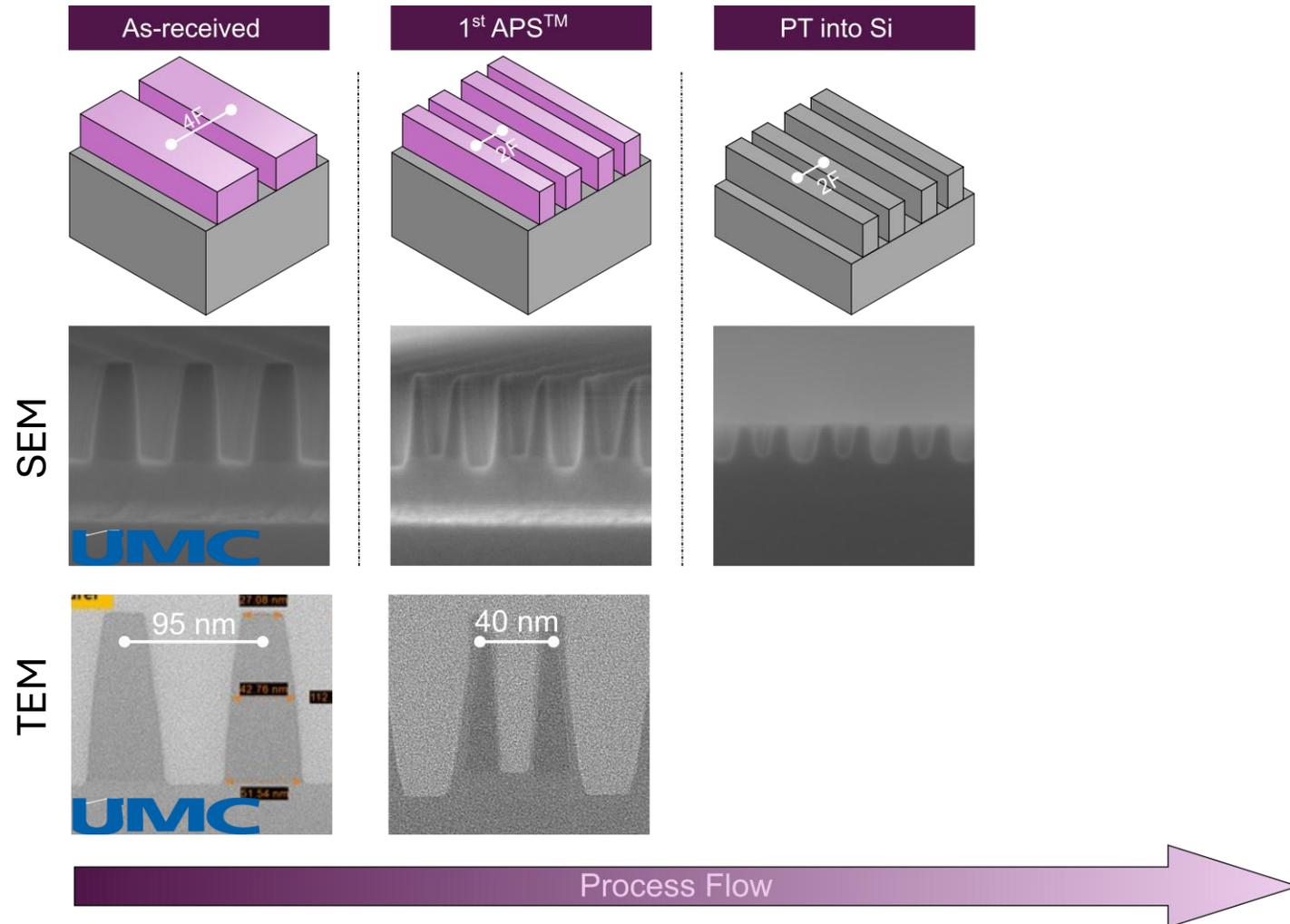
# Simplifying Quadruple Patterning by APS™



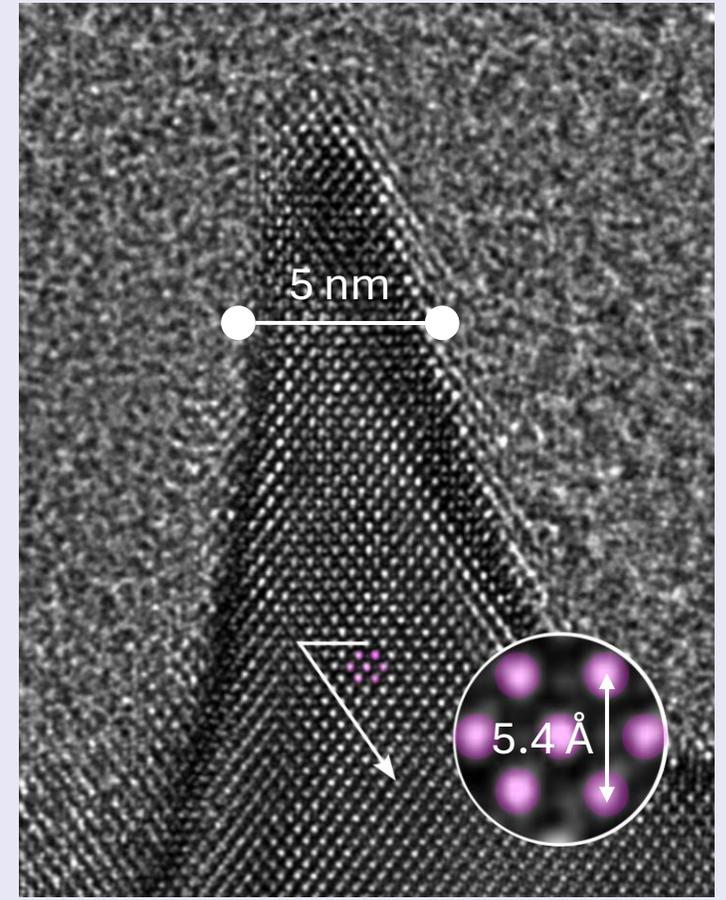
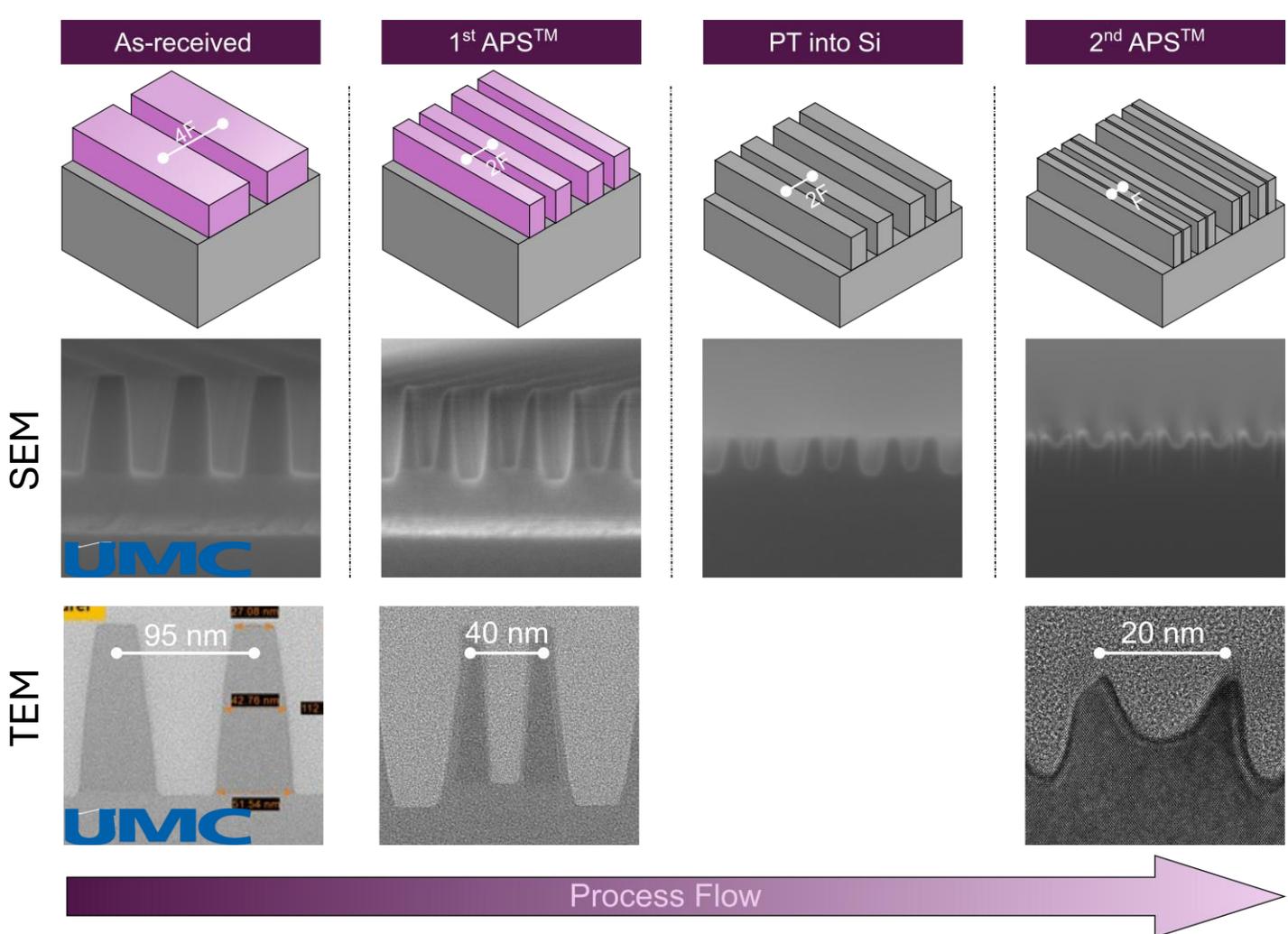
# Simplifying Quadruple Patterning by APS™



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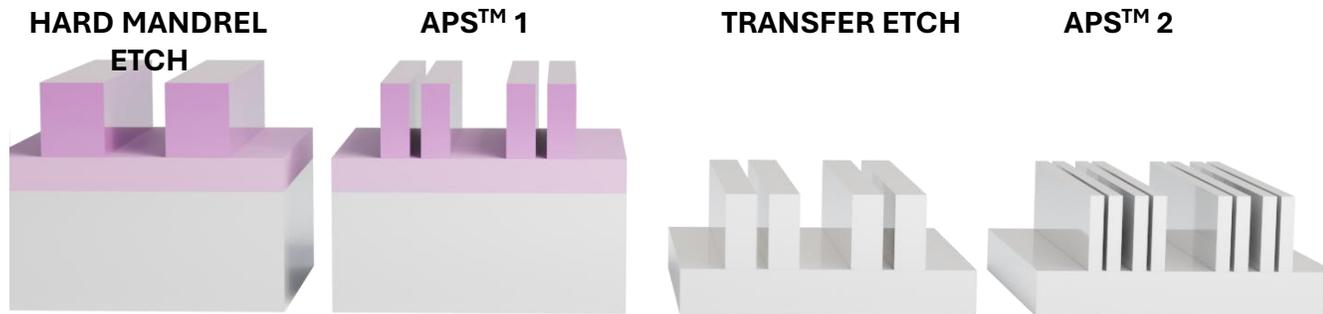
# Comparing SAQP with APS™

## Simplified SAQP Process Flow



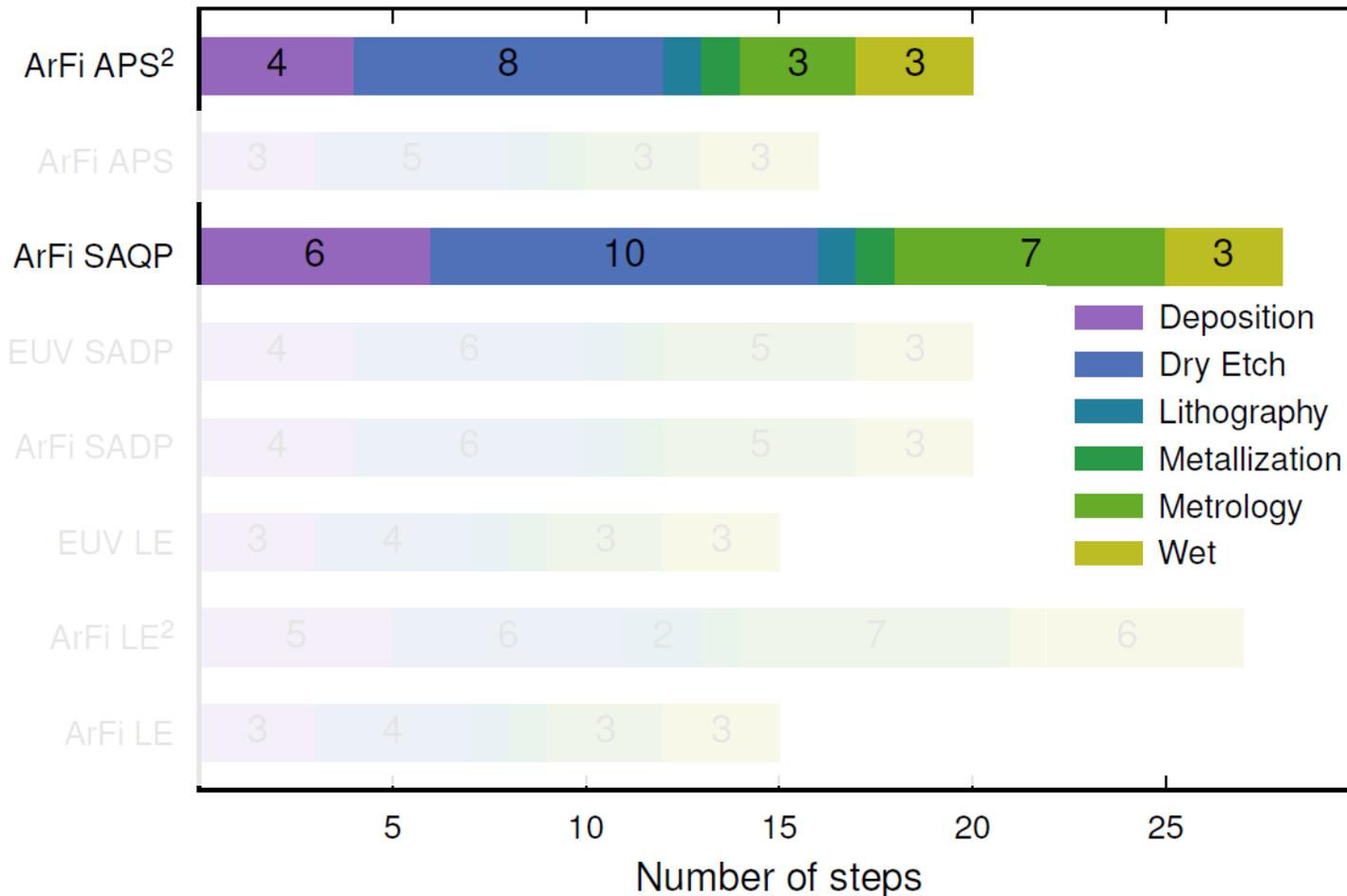
*E. Altamirano-Sánchez et al, SPIE Newsroom (2016)*

## APS™ Pitch Quartering



- No deposition steps required.
- No additional intermittent hard masks needed.
- Improved control over CD and pitch walk.

# Process Simplification Achieved Using APS™



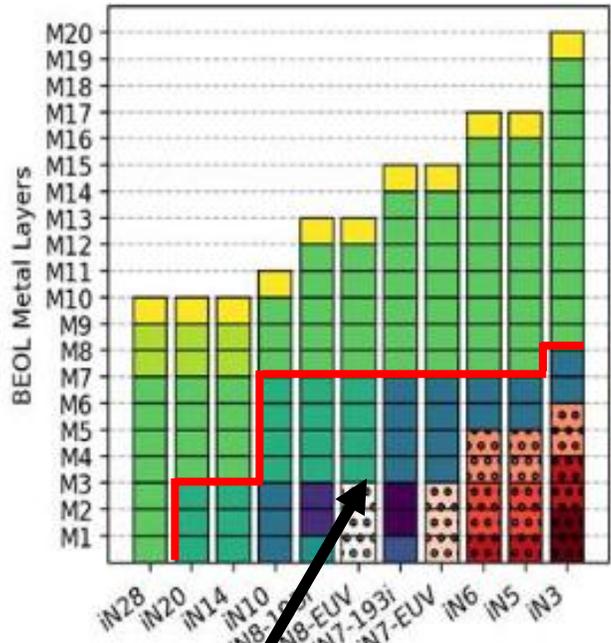
- Several different multiple patterning approaches exist.
- Litho passes are expensive, SADP/SAQP schemes become attractive as only one litho pass is required. Removes overlay concerns.
- However, pitch walk is incredibly hard and costly to control in SAQP.
- APSTM allows for significant reduction in process complexity compared to SAQP:
  - No deposition required (2 steps + metrology)
  - No intermediate HM for structural stability needed.

# APS™ for Greener Semiconductors



**APS:**  
**A**tomic  
**L**ayer  
**E**tching  
**P**itch  
**S**plitting

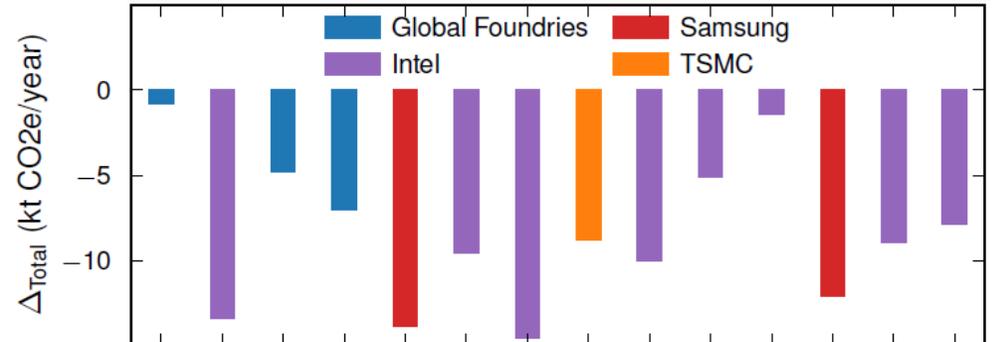
## APS™ Applications



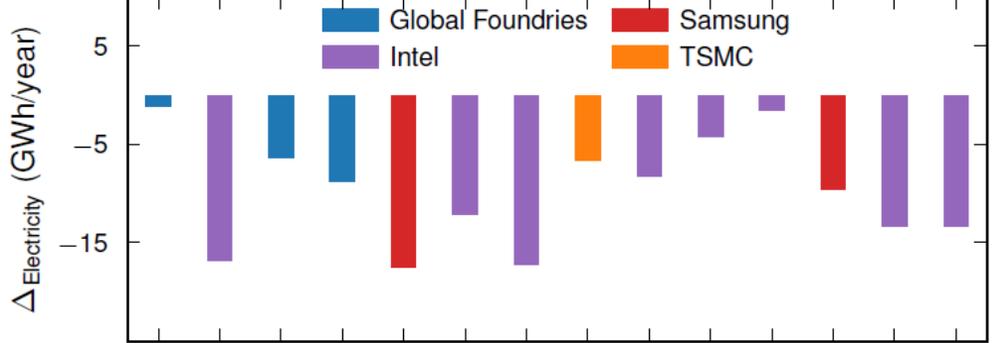
M. Garcia Bordon et al., IEDM 2020.

Multiple patterning implementation region.

## CO2eq Savings



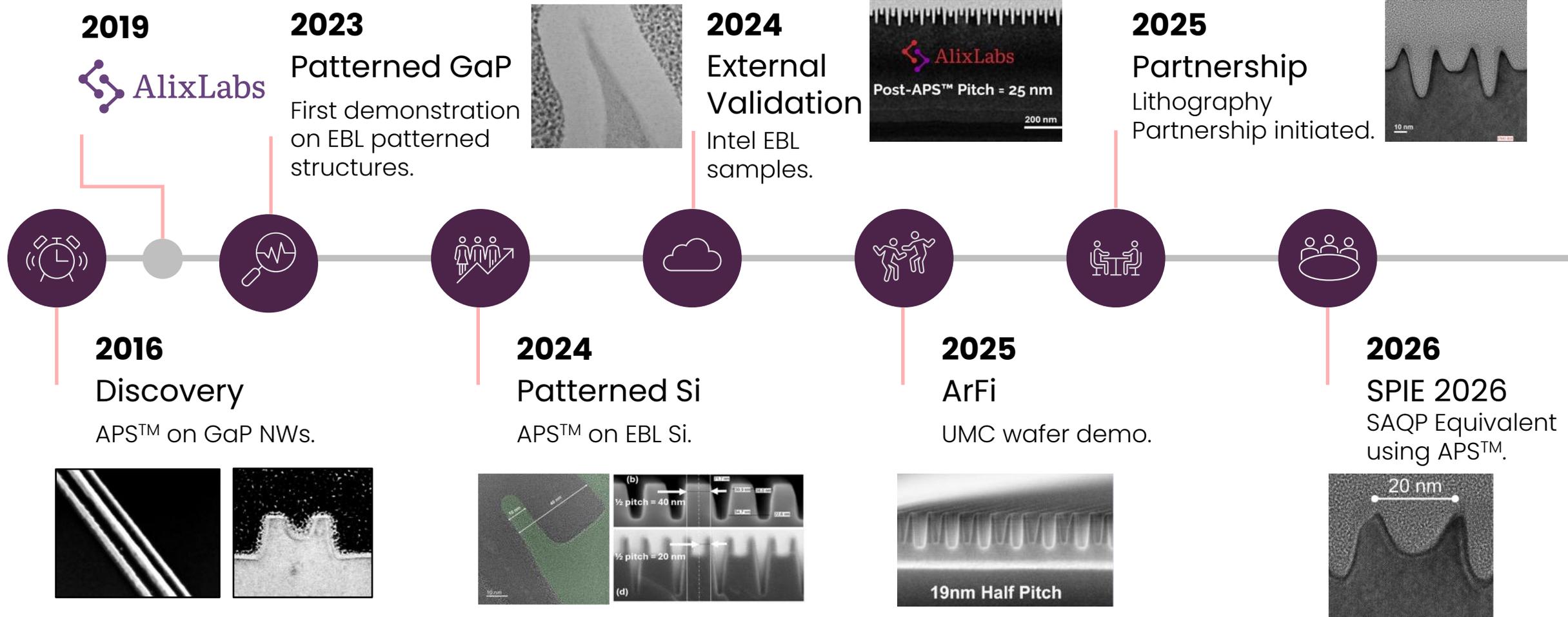
## Electricity Savings



N14 (Germany)  
 N14 (US)  
 N14 (US)  
 N12 (US)  
 N11 (Texas)  
 N10 (Oregon)  
 N7 (US)  
 N4 (Arizona)  
 N4 (Ireland)  
 N4 (Oregon)  
 N3 (Ireland)  
 N3 (Texas)  
 A18 (Arizona)  
 A18 (Oregon)

\*Data from Tech Insights open source database. Manuscript in preparation.

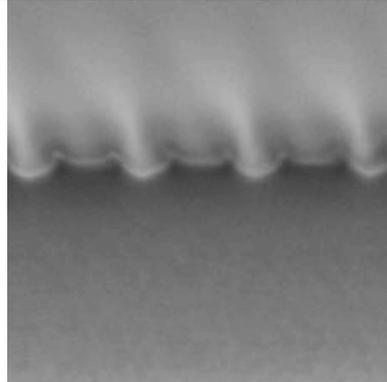
# APST<sup>TM</sup> Development Timeline



# APS™ Outlook – New Applications

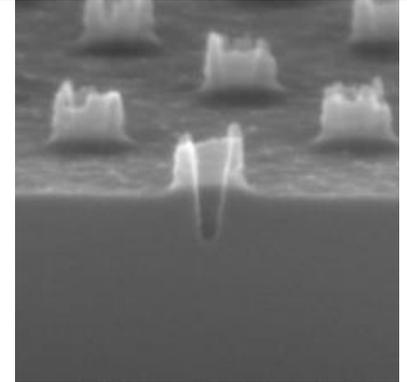
**2026**  
Hard Masks

APS™ on hard mask

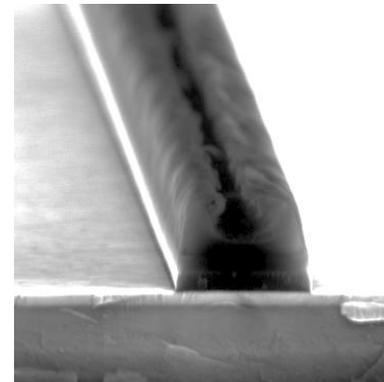


**2026**  
Vias

APS™ on vias.



**2026**  
Photoresist  
APS™ on resists.



# AlixLabs APS™ & ALE Equipment

## Alpha



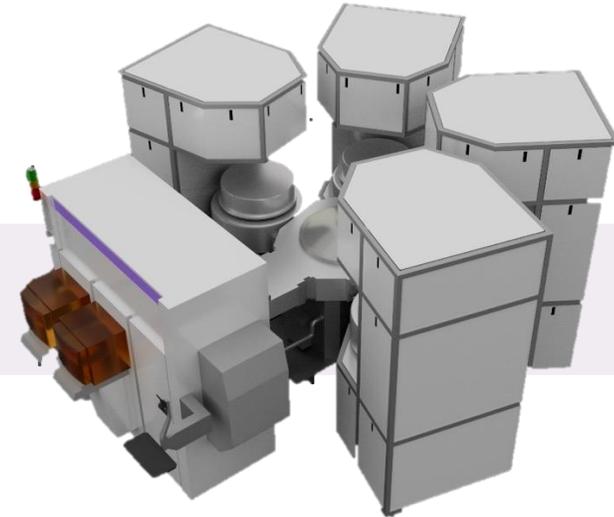
300 mm wafer capabilities.  
Available for demos.

## Beta



Cluster tool with multiple chamber  
processing and automatic handling.  
Ready in Q3 2026.

## Gamma



Gamma platform  
Production ready HVM.  
(conceptual design)

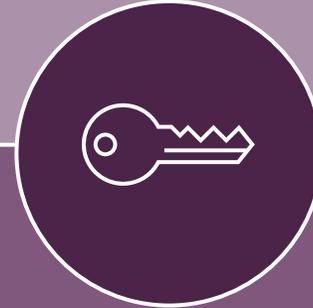
# Concluding Remarks



Costs and complexity in advanced nodes are largely driven by complex patterning processes.



APST<sup>™</sup> offers a new approach of accessing advanced process nodes without investing in new lithography.



APST<sup>™</sup> can reduce cost and complexity while improving yield when compared to SADP and SAQP.



APST<sup>™</sup> has the potential to lower CO<sub>2</sub>eq emissions and reduce electricity consumption for more sustainable fabrication!



Alix Labs

