Atomic Layer Etching Pitch Splitting (APS^{TM}) for Nanoimprint Lithography - Combining Simplicity, Precision, and Sustainability

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ABSTRACT

Atomic Layer Etching Pitch Splitting (APS^{TM}) is a scalable and cost-efficient approach for high-resolution pattern multiplication. In this work, APS^{TM} is combined with Nanoimprint Lithography (NIL) to enable low-cost, sustainable fabrication of dense silicon nanostructures with atomic-scale precision. Line/space patterns with an initial half-pitch of 26 nm were defined by NIL, transferred into silicon, and subsequently pitch-split using APS^{TM}. The process yielded silicon lines with a critical dimension of 10 nm and a half-pitch of 12 nm, while maintaining good structural integrity and low line edge roughness (LER) of 1.7 nm.

Keywords: APS^{TM}, ALE, Atomic Layer Etching, Self-Aligned Quadruple Patterning, SAQP, Atomic Scale Processing, Multiple Patterning

INTRODUCTION

Atomic Layer Etching Pitch Splitting (APS^{TM}) is a process to develop dense patterns on wafers while at the same time being a scalable and cost-efficient alternative to conventional pitch-splitting techniques such as self-aligned double patterning (SADP) or Litho-Etch-Litho-Etch (LELE). In our previous works [1-3], we demonstrated APS^{TM} for various patterns and material systems. Specifically, we applied the APS^{TM} process to GaP nanowires, randomly distributed on silicon surfaces, as well as on lithographically defined patterns using electron beam lithography (EBL) on both GaP and Si structures, including features fabricated on 300 mm silicon wafers. These studies highlighted the potential of APS^{TM} as a single-step process with atomic-scale control for pattern pitch multiplication. In this study, we extend the work by demonstrating APS^{TM} on nanostructures defined using Nanoimprint Lithography (NIL). NIL has emerged as a promising candidate for low-cost, high-throughput patterning, and presents an alternative to traditional projection lithography. By combining APS^{TM} with NIL, we aim to enforce the cost-effectiveness and scalability of both techniques, leveraging NIL for low-cost pattern definition and APS^{TM} for atomic-level precision and pattern fidelity. Using this approach, we address multiple key challenges in advanced semiconductor manufacturing.

METHOD

Nanoimprint Lithography (NIL) was used to define periodic line/space (L/S) features with an initial half-pitch (HP) of 26 nm on a NIL resist layer. The patterned resist was then used as a mask for subsequent pattern transfer (PT) into the silicon substrate. The process involved the use of a residual layer removal step followed by an anisotropic silicon etch. Following NIL, the pattern was transferred from the resist into the silicon substrate through a conventional inductively coupled plasma reactive ion etching (ICP-RIE) process. Using O_2 plasma, a descum process was applied to reveal the Si surface, then the pattern was transferred into Si using a Fluorine based process and as a last step the remaining resist was cleaned using O2 plasma. Figure 1 a-d) illustrates this sequence, showing the progression from NIL resist patterns, through silicon pattern transfer, to the final structure, prior to the APS^{TM} step. After successful transfer of the initial features into silicon, the APS^{TM} process was applied to split the silicon lines, effectively doubling the initial pattern density.

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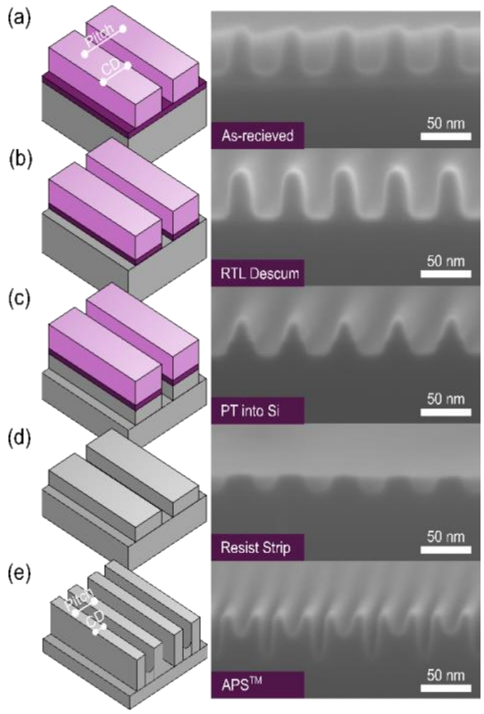

Figure 1: a)-e) Process flow showing pattern transfer from NIL resist down to silicon substrate and APS™, including cross-sectional SEM images of a) pattern after NIL, b) removing resist residues using O_2 plasma, c) pattern after transferring to the Si substrate, d) resist striping in a O_2 plasma process and e) after APS™ demonstrating a 12 nm half pitch for 10 nm structures.

RESULTS & DISCUSSION

Figure 1-e) shows cross-sectional SEM images of silicon lines after APS™ processing, showing clear pitch splitting with well-preserved sidewall profiles. The application of APS™ to NIL-defined structures yielded sub-12 nm half-pitch features with good structural integrity and minimal roughness. The final line critical dimension (CD) after APS™ was 10 nm with half pitch of 12 nm.

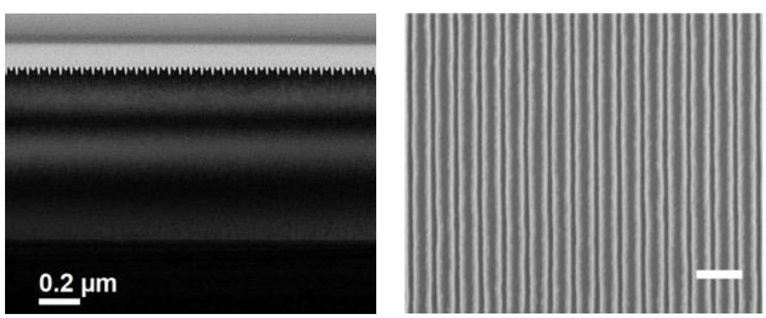

Figure 2: Left) TEM image of APS™-processed structures. Right) top-view image of the structures used for line-edge roughness measurement. The scale bar is 100nm.

Figure 2-left depicts high-resolution transmission electron microscopy (TEM) to visualize split of the silicon structures. The TEM image confirms successful splitting of the silicon features and demonstrates the stability and robustness of the APS™ process. Measurements of line edge roughness (LER) showed an average value of 1.72 nm, confirming high pattern fidelity and the capability of APS™ to maintain low variability even at this scale. By minimizing the number of nanofabrication steps, the combined APS™ + NIL approach offers a simplified, and sustainable patterning solution—aligning well with industry demands for greener and more

affordable semiconductor manufacturing. This integration leverages NIL for large-area, low-cost, high throughput pattern definition and APS™ for precise pitch scaling and resolution enhancement. Together, they enable Si nanostructures with a CD of 10 nm and half pitch of 12 nm, with controlled LER, which are critical for performance and yield in leading-edge logic and memory devices. The compatibility of APS™ with NIL further strengthens its potential for high-throughput production, particularly in scenarios where conventional EUV-based patterning may not be economically viable.

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