Self-Aligned Quadruple Patterning Made Simple – Extending the Applications of Atomic Layer Etch-induced Pitch Splitting (APS^{TM})

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ABSTRACT

We extend the applications for our atomic layer etch-induced pitch splitting (APS^{TM}) process, positioning it as an alternative to self-aligned quadrupole patterning (SAQP). The implementation of APS^{TM} enables a process flow with only three steps to achieve a 4x density increase of the initial line features. This is achieved by using the result of the initial APS^{TM} as a split mask for pattern transfer into the underlaying Si substrate, after which a second APS^{TM} step is carried out. Using this approach, we reduce the half pitch (HP) and critical dimension (CD) from 47.5 nm and 52 nm to 12 nm (average) and 12 nm respectively, corresponding to a 4x and 4.3x improvement.

Keywords: APS^{TM}, ALE, Atomic Layer Etching, Self-Aligned Quadruple Patterning, SAQP, Pitch Splitting, Atomic Scale Processing, Cost-effective Multiple Patterning

INTRODUCTION

To advance cost-effective sub-20-nm feature patterning, we have developed atomic layer etch-induced pitch splitting (APS^{TM}), a new and alternative process approach to multiple patterning methods such as Self-Aligned Double/Quadruple Patterning (SADP/SAQP) and Litho-Etch-Litho-Etch (LELE). APS™ incorporates self-limiting processes into existing nanofabrication workflows, enabling selective removal of material from pre-patterned features[1,2]. This eliminates the need for multiple lithography, deposition, and etching cycles that are usually required in conventional pitch-splitting approaches. This significantly reduces process complexity providing superior precision and patterning fidelity, key to defining critical on-device features. We recently demonstrated APS^{TM} as an alternative to SADP, enabling a 2x increase in line density when compared to post lithography[3]. Using APS^{TM}, features with critical dimension (CD) below 15 nm and a sub 15 nm half-pitch were demonstrated in single crystalline silicon. In this work, we extend the applications of APS^{TM} by going one step further, increasing the initial line density by 4x (4F → F architecture), positioning it as a new alternative to SAQP.

METHODS

APS^{TM} was performed on production-grade 300 mm single crystalline silicon wafers provided by our partner United Microelectronics Corporation (UMC). The initial test structures comprised patterned amorphous silicon (aSi) features with a starting critical dimension (CD) of 52 nm and a half-pitch (HP) of 47.5 nm. To achieve a 4x increase in line density a sequential process flow was implemented: (1) an initial APS™ step was applied to selectively split the aSi features, doubling the line density; (2) the resulting pattern was transferred into the bulk Si substrate via anisotropic reactive ion etching using a chlorine based chemistry; and (3) a second APS™ step was performed directly on the substrate features to achieve the final quadruple density. Pattern fidelity and dimensional scaling were characterized throughout the process steps using high-magnification top-down and cross-section Scanning Electron Microscopy (SEM).

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RESULTS & DISCUSSION

Figure 1 shows the process flow implemented from post-lithography to the final structure with 4x increase in line density. The process flow starts with an initial APS^{TM} step to split the patterned aSi features (Fig. 1a), achieving a 2x increase in line density (Fig. 1b). These features are then transferred into the Si substrate as a second step (Fig. 1c). After the features are transferred to the Si substrate, a second APS^{TM} step is implemented, yielding a 4x increase in line density as compared to the initial pattern (Fig. 1d). Figure 2 shows high magnification SEM images comparing the initial (Fig. 2a) and final pattern (Fig. 2b). Using the described approach, patterns with an average half pitch (HP) of ~12 nm and CD of ~12 nm are achieved, corresponding to a ~4x and ~4.3x improvement compared to the 47.5 nm HP and 52 nm CD of the initial pattern.

APS^{TM} enables a substantial reduction in process complexity while achieving similar results as more traditional multiple patterning techniques such as SAQP. The reduced process complexity should provide a significant improvement in variability, and thereby the yield of leading-edge processes, a pronounced challenge when implementing traditional SAQP.

This work extends the applications of APS^{TM}, positioning it as a compelling alternative for multiple patterning processes with lower process complexity. Additionally, the removal of additional deposition and lithography steps significantly reduces the operating cost and capital expenditures, making it a more sustainable solution to meet industry demands for time, manageable investments, and resource conservation as well as reduced CO$_2$eq emissions.

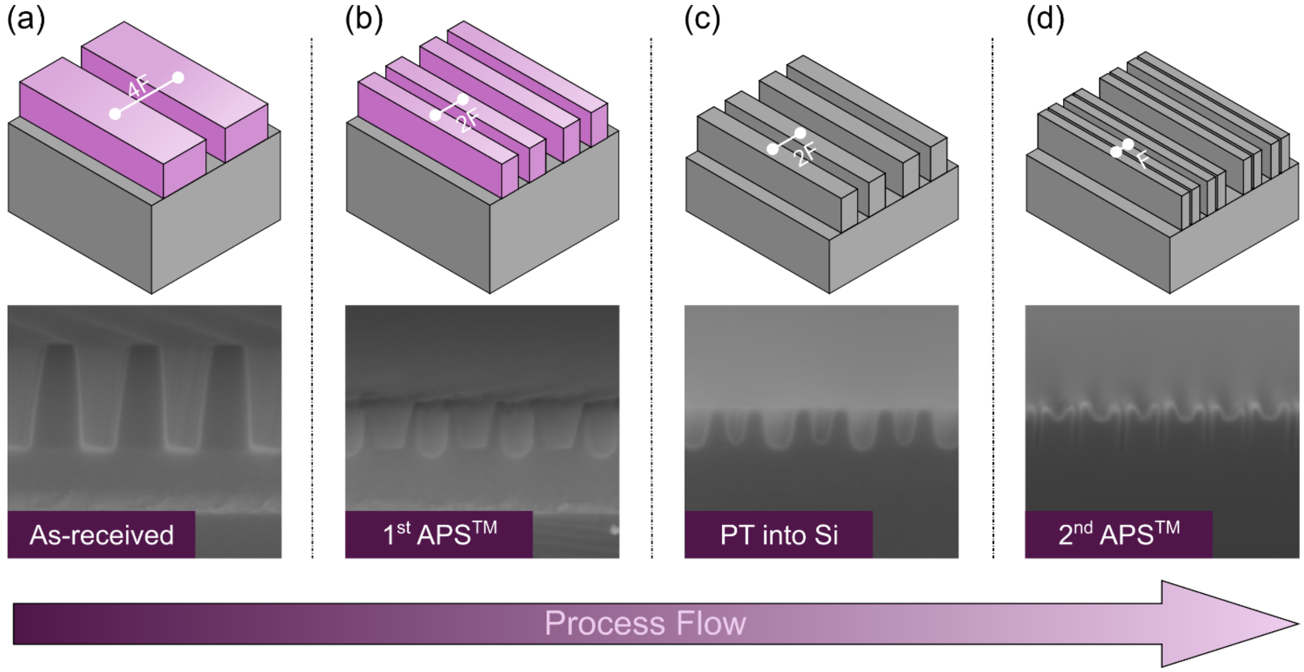

Figure 1. Three step process flow using APS^{TM} to increase the line feature-density by a factor of 4x. (a) Production grade immersion lithography sample as prepared by UMC, with a feature size of 4F. (b) First APS^{TM} split, which doubles the line density, yielding a feature size of 2F. (c) The split pattern in (b) is used as a transfer mask into the Si substrate underneath, keeping the same line density and feature size of 2F. (d) A second APS^{TM} step is implemented to split the Si substrate and double the line density by another 2x, resulting in a 4x increase in line feature density and a final feature size of F.

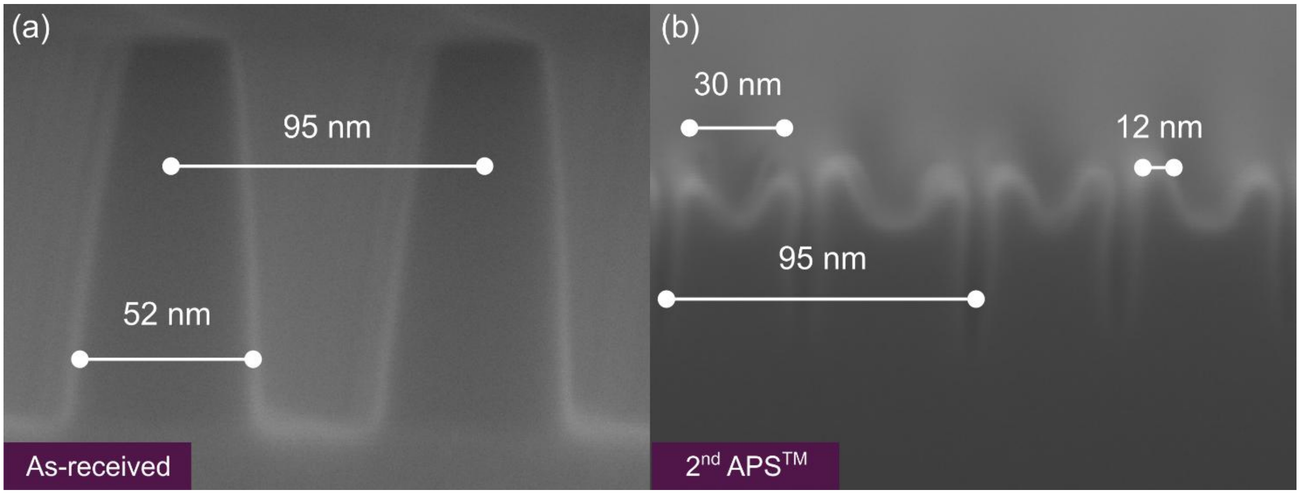

Figure 2. Comparison of the initial features on the 300 mm production grade immersion lithography wafer versus those after the three-step process flow involving two APS^{TM} steps. (a) shows the initial features post lithography, having a CD of 52 nm and a HP of 47.5 nm. In (b) the final structure is presented where a 4x increase in the line density is achieved. The final HP (average) and CD achieved is ~12 nm and ~12 nm respectively, corresponding to a ~4x and ~4.3x improvement.

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